METHOD OF FORMING A VERTICAL DOUBLE GATE SEMICONDUCTOR DEVICE AND STRCTURE THEREOF

Abstract of the Disclosure

A vertical double gate semiconductor device (10) having separate, non-contiguous gate electrode regions (62, 64) is described. The separate gate electrode regions can be formed by depositing a gate electrode material (28) and anisotropically etching, planarizing or etching back the gate electrode material to form the separate gate electrode regions on either side of the vertical double gate semiconductor device. One (66) or two (68, 70) contacts are formed over the separate gate electrode regions that may or may not be electrically isolated from each other. If formed from polysilicon, the separate gate electrode regions are doped. In one embodiment, the separate gate electrode regions are doped the same conductivity. In another embodiment, an asymmetrical semiconductor device is formed by doping one separate gate electrode region n-type and the other separate gate electrode region p-type.